OSD-2828OGDEDF01

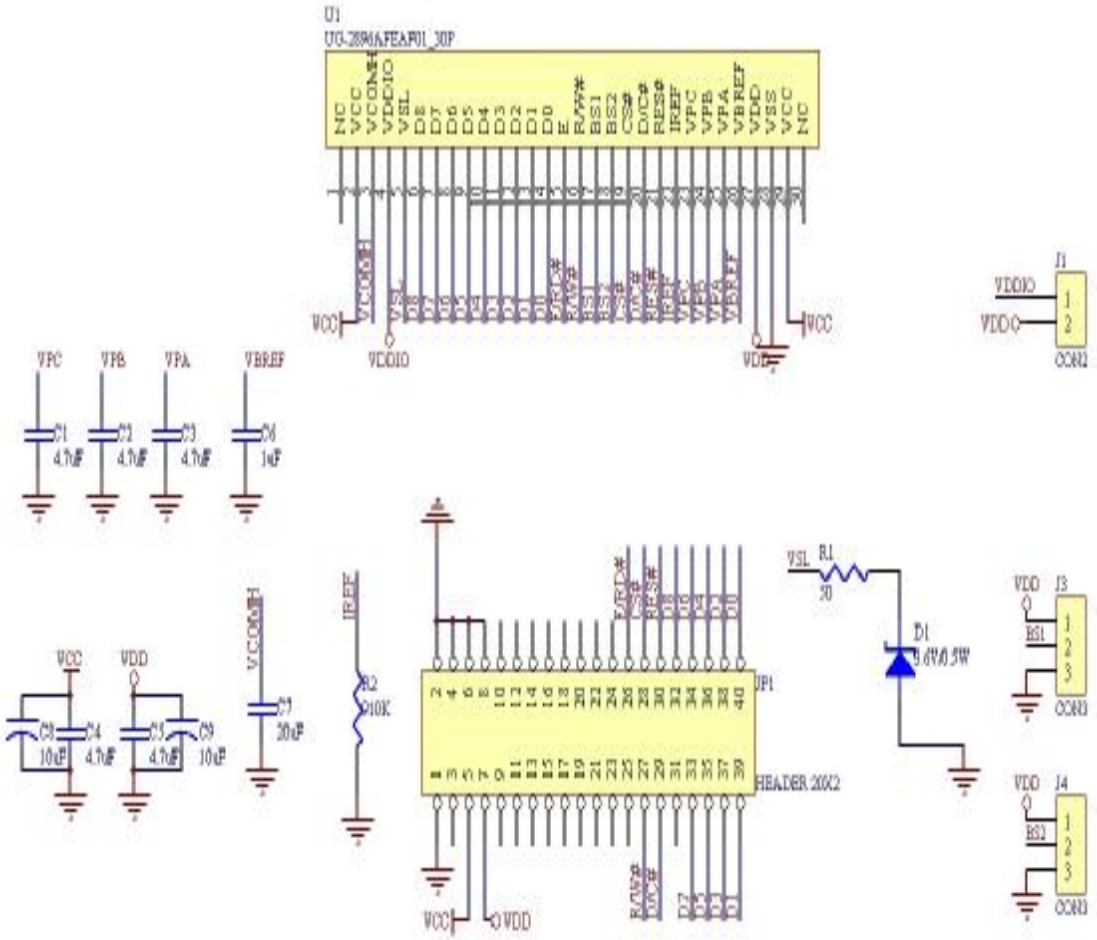
Application note

Evaluation Kit User Guide

REVISION HISTORY

Date	Page	Contents	Version
2005/09/23		Preliminary	Preliminary

EVK Schematic



Symbol define

D0-D8：These pins are 9-bit bi-directional data bus to be connected to the MCU's data bus.

BS1,BS2,BS3：These input pins are used to configure MCU interface selection by appropriate logic setting, which is described in the following table. User can fixed these pins by jump (J3, J4). Unlike BS0~2 are can control by hardware, **BS3 is control by software command 0xA0 only**.**BS0 has already fixed to GND.**

	6800-parallel interface (8 bit)	8080-parallel interface (8 bit)	6800-parallel interface (16 bit)	8080-parallel interface (16 bit)	Serial interface
BS0	0	0	1	1	0
BS1	0	1	0	1	0
BS2	1	1	1	1	0
BS3	0	0	0	0	0

	6800-parallel interface (9 bit)	8080-parallel interface (9 bit)	6800-parallel interface (18 bit)	8080-parallel interface (18 bit)
BS0	0	0	1	1
BS1	0	1	0	1
BS2	1	1	1	1
BS3	1	1	1	1

Table 1 – MCU Interface Selection Setting

E/RD#：This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the chip is selected.

When connecting to an 8080-microprocessor, this pin receives the Read (RD) signal. Data read operation is initiated when this pin is pulled low and the chip is selected. When serial interface is selected, this pin E(RD) must be connected to VSS.

R/W#：This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin will be used as Read/Write (R/W) selection input. Read mode will be carried out when this pin is pulled high and write mode when low.

When 8080 interface mode is selected, this pin will be the Write (WR) input. Data write operation is initiated when this pin is pulled low and the chip is selected. When serial interface is selected, this pin R/W must be connected to VSS.

D/C#：This pin is Data/Command control pin. When the pin is pulled high, the data at D0-D17 is

treated as display data. When the pin is pulled low, the data at D0-D17 will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the timing characteristics diagrams at following pages and datasheet.

RES#：This pin is reset signal input. When the pin is low, initialization of the chip is executed.

CS#：This pin is the chip select input. The chip is enabled for MCU communication only when CS is pulled low.

VCC：This is the most positive voltage supply pin of the chip.

VDD：Power supply pin for logic operation of the driver.

GND：Power supply ground.

VDD = 2.4 to 3.5V, TA = -40 to 85°C

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Table 2 6800-Series MPU Parallel Interface Timing Characteristics

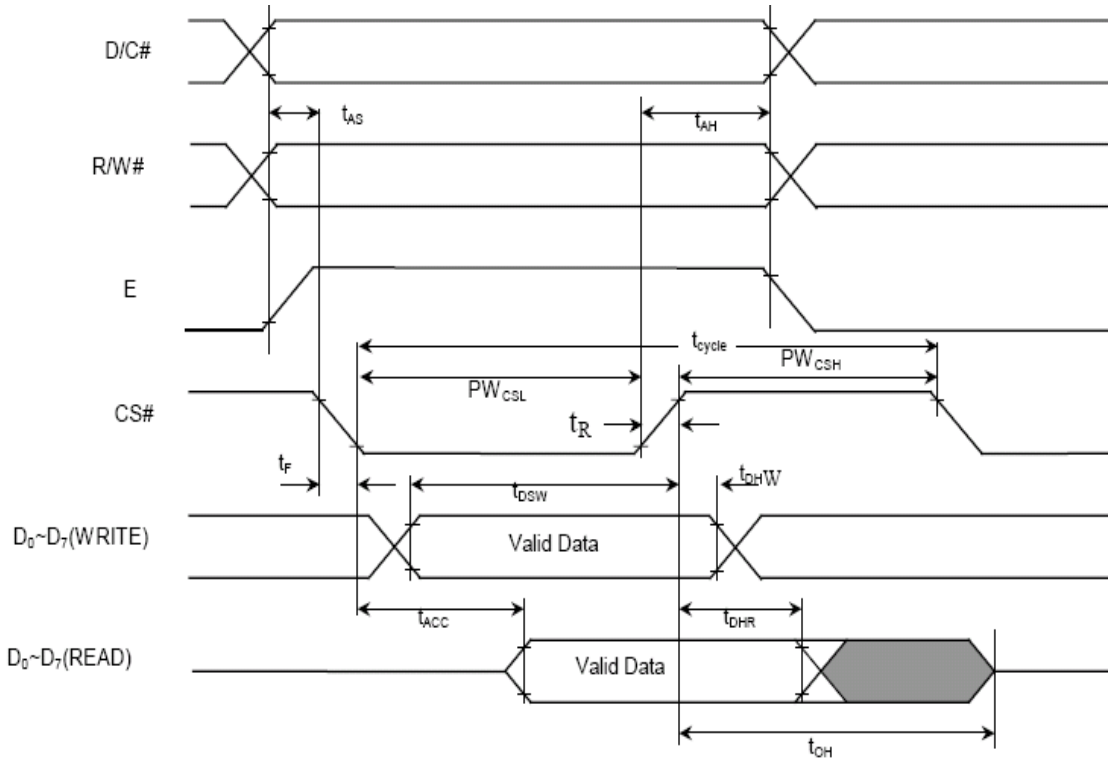


Figure 1 6800-series MPU parallel interface characteristics

Note：When 9 bit used: D_0 ~ D_8 instead.

VDD = 2.4 to 3.5V, TA = -40 to 85°C

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Table 3 8080-Series MPU Parallel Interface Timing Characteristics

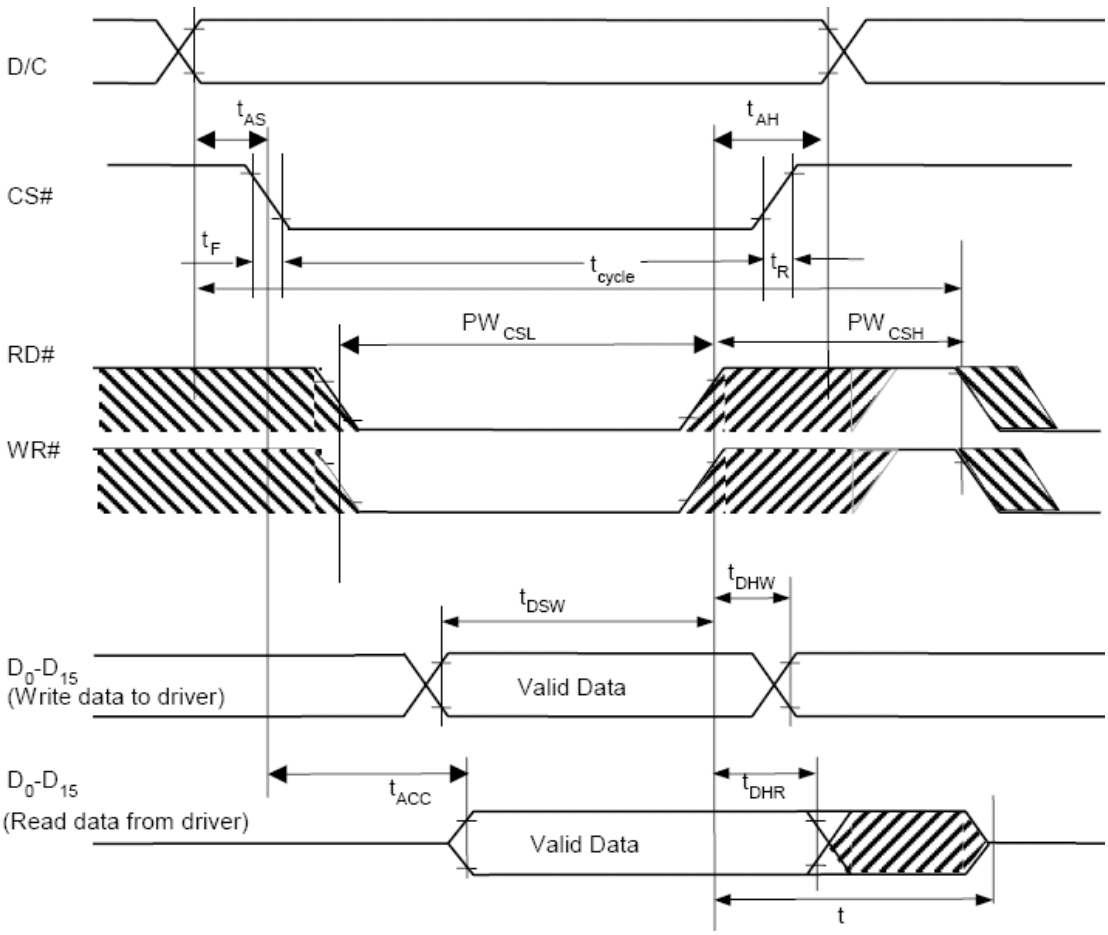


Figure 2 8080-series MPU parallel interface characteristics

Note：When 9 bit used: D_0 ~ D_8 instead.

VDD = 2.4 to 3.5V, TA = -40 to 85°C

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	100	-	-	ns
t_{DHW}	Write Data Hold Time	100	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Table 4 Serial Interface Timing Characteristics

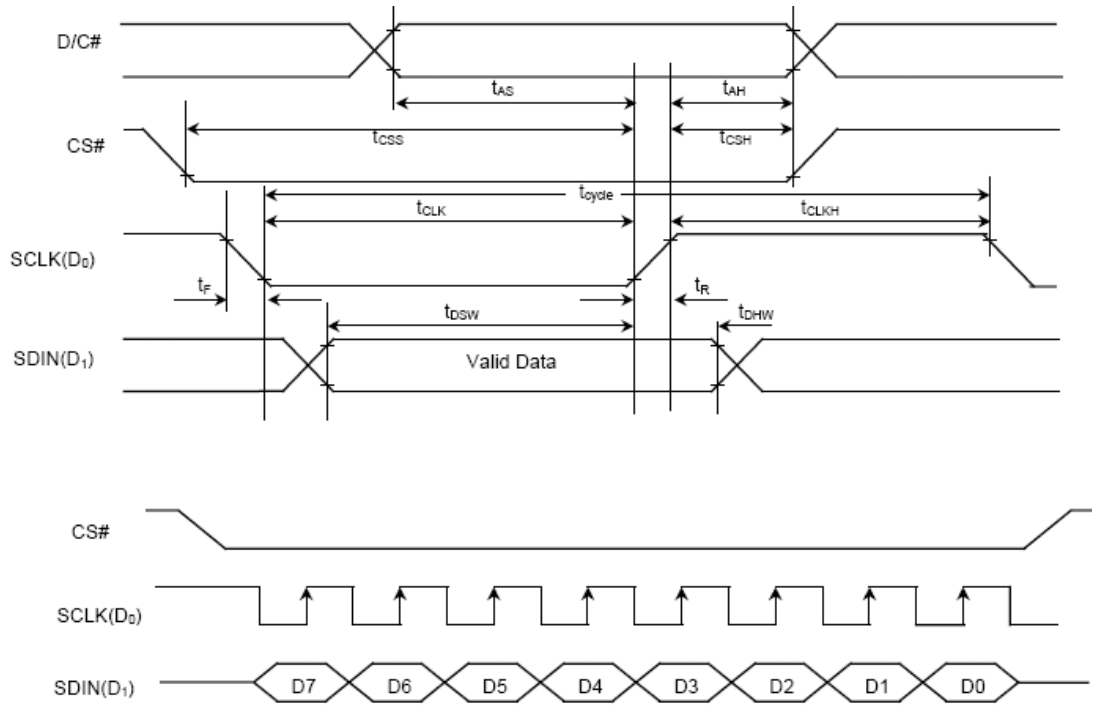


Figure 3 Serial interface characteristics

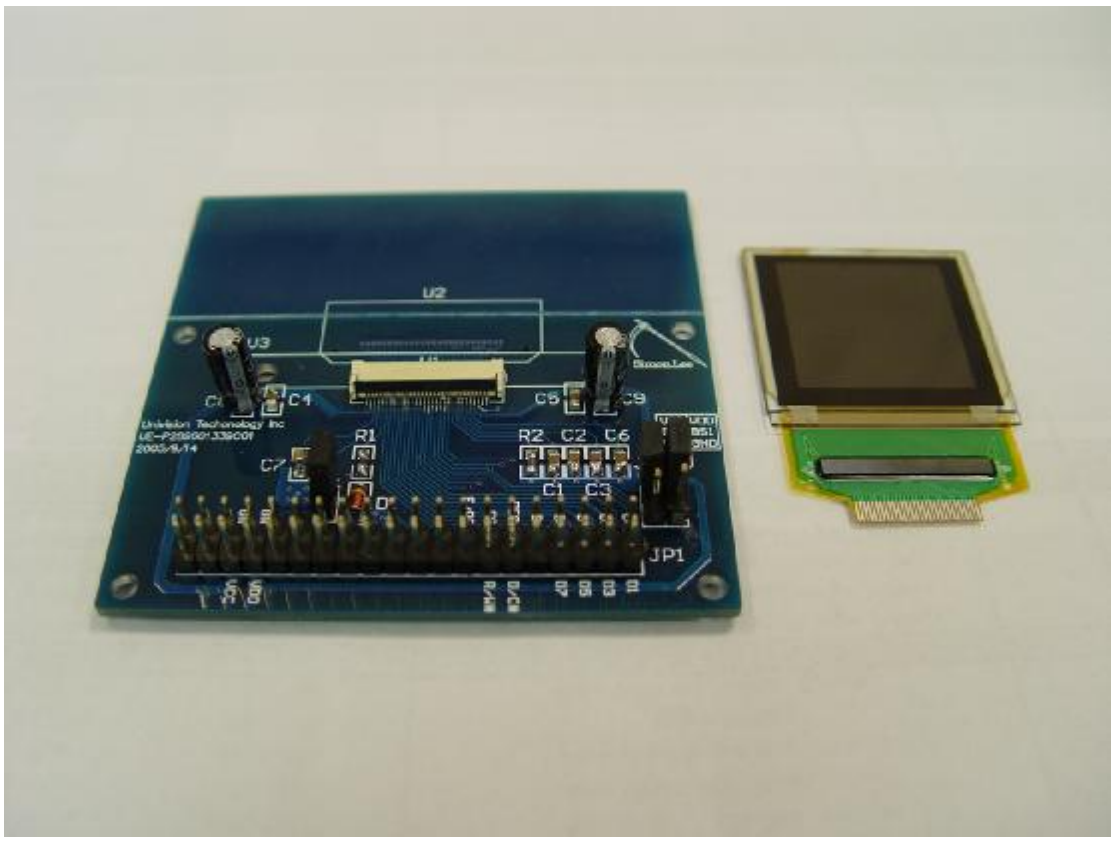


Figure 4 EVK PCB and OLED Module

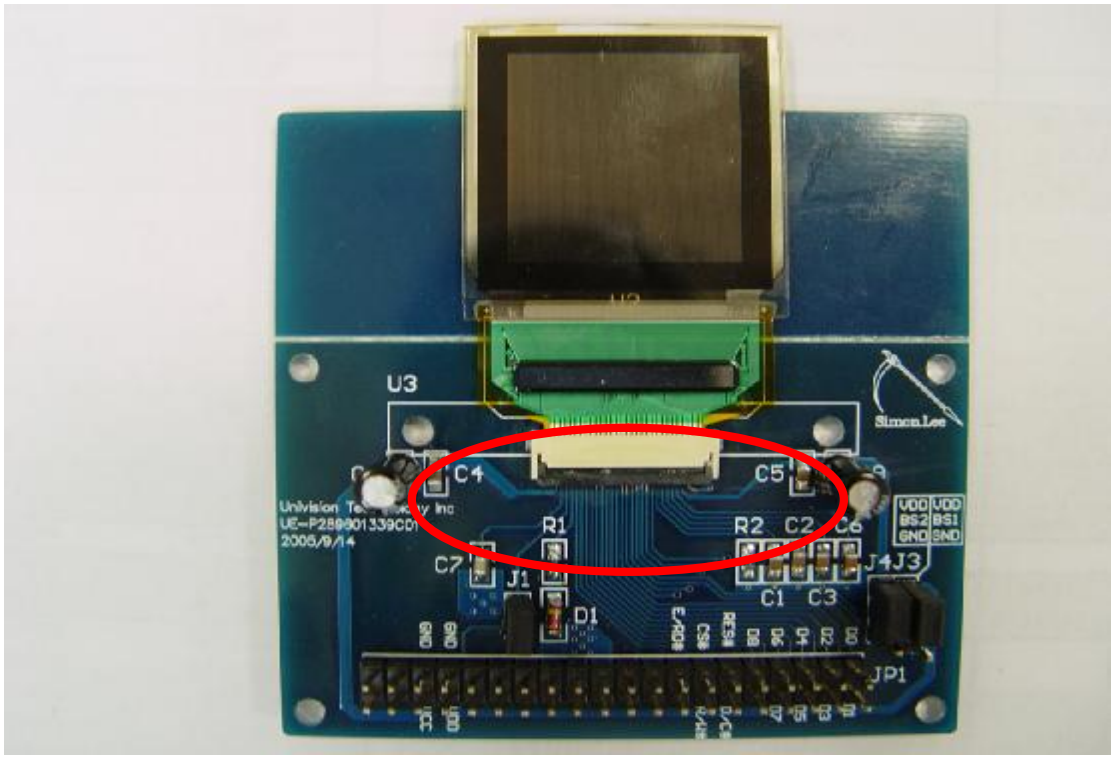


Figure 5 the module and EVK assembled (Top view)

Because the package of OSD-2828OGDEDF01 is COF, that the connect pads are on the top of the module, and the connector which on the EVK PCB board is double size connect type. So when assemble the module with EVK. The module must face up first and plug into the connector. When finished assembled the module and EVK, then push the locking pad to lock the module. See the figure 5.

When finished assembled the module and EVK. User can use leading wire to connect EVK with customer's system. The example shows as figure 6.

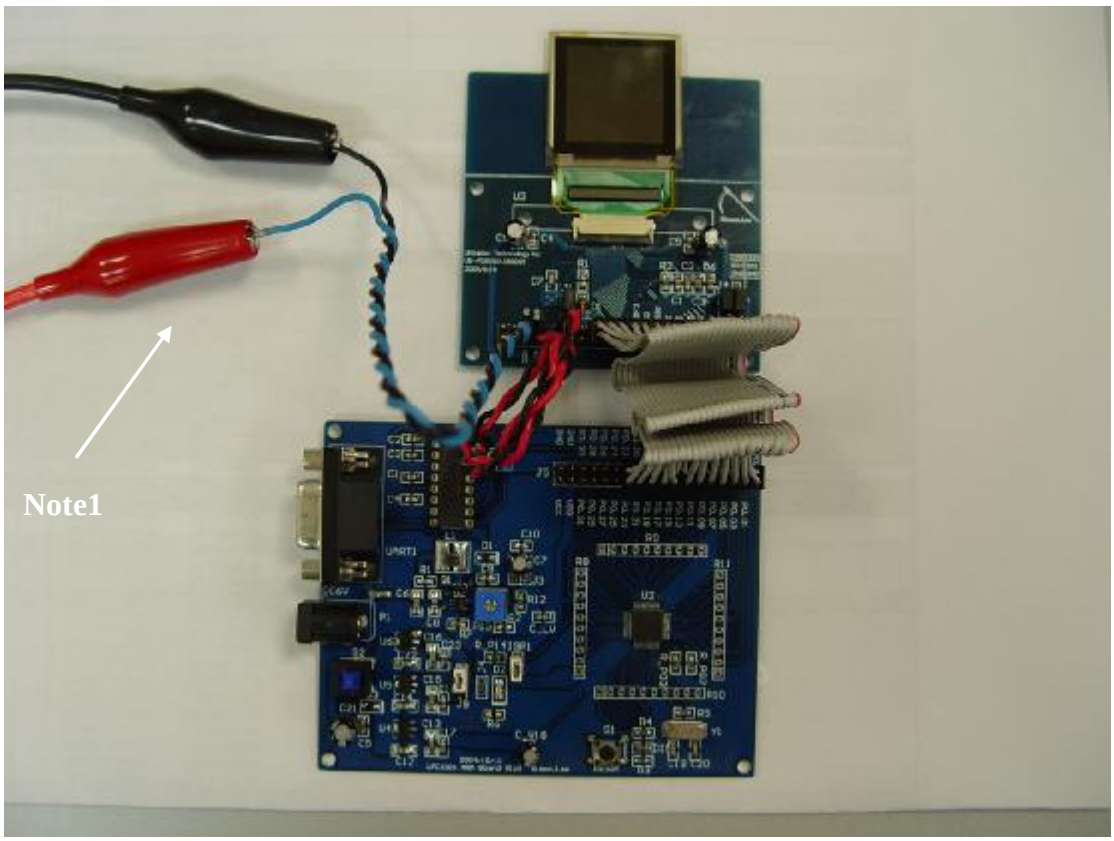
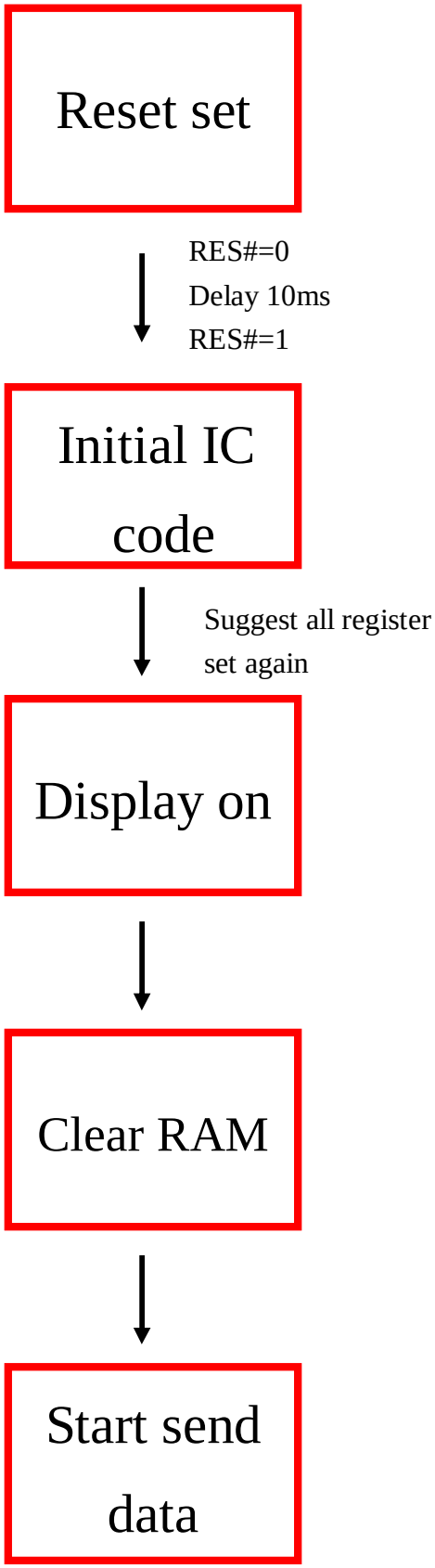


Figure 7 control MCU connect with EVK

Note 1：It is the external most positive voltage supply. In this sample is connected to power supply.

How to use OSD-2828OGDEDF01



RD recommends Initial Code:

```
void Initial_ic(void)
{
	IOCLR=0xffffffff;		//data=0
	IOSET=bE_RD;
	IOCLR=bD_C|bR_W|bCS;
	Reset_SSD1339();

	write_c(0xa0);		// Set Re-map / Color Depth
	write_d(0xb4);		// 262K 8bit	R->G->B
	write_c(0xa1);		// Set display start line
	write_d(0x00);		// 00h start
	write_c(0xa2);		// Set display offset
	write_d(0x80);		// 80h start
	write_c(0xA6);		// Normal display
	write_c(0xad);		// Set Master Configuration
	write_d(0x8e);		// DC-DC off & external VcomH voltage & external	pre-charge voltage
	write_c(0xb0);		// Power saving mode
	write_d(0x05);
	write_c(0xb1);		// Set pre & dis_charge
	write_d(0x11);		// pre=1h dis=1h
	write_c(0xb3);		// clock & frequency
	write_d(0xf0);		// clock=Divser+1	frequency=fh
	write_c(0xbb);		// Set pre-charge voltage of color A B C
	write_d(0x1c);		// color A
	write_d(0x1c);		// color B
	write_d(0x1c);		// color C
	write_c(0xbe);		// Set VcomH
	write_d(0x1f);		//
	write_c(0xc1);		// Set contrast current for A B C
	write_d(0xaa);		// Color A
	write_d(0xb4);		// Color B
	write_d(0xc8);		// Color C
	write_c(0xc7);		// Set master contrast
	write_d(0x0f);		// no change
	write_c(0xca);		// Duty
	write_d(0x7f);		// 127+1
	write_c(0xaf);		// Display on
}

void Reset_SSD1339(void)
{
	IOCLR=bRES;
	Delay_1ms(100);
	IOSET=bRES;
}

void write_c(unsigned char out_command)
{
	IOCLR=bD_C;
	IOCLR=bCS;
	IOCLR=bR_W;
	IOCLR=0x000000ff;
	IOSET=out_command;
	IOSET=bR_W;
	IOSET=bCS;
	IOSET=bD_C;
}
```

```
void write_d(unsigned char out_data)
{
        IOSET=bD_C;
        IOCLR=bCS;
        IOCLR=bR_W;
        IOCLR=0x000000ff;
        IOSET=out_data;
        IOSET=bR_W;
        IOSET=bCS;

}

void Delay_1ms(int Cycle)
{
unsigned int i,k;
        for (i=0 ;i<Cycle;i++)
                for(k=0;k<0x5fff;k++);
}
```

∗write_c= Write Command , write_d= Write Data